A Modulation Method for DC-Link VoltageBalancing Control of a T-Type Converter

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Abstract— In this paper, an innovative method for DC-link voltage balancing in a T-type converter is proposed. The proposed method uses a single voltage sensor to sense one of the capacitor voltages. This method possesses the advantages of lesser number of auxiliary components to balance the DC-link capacitor voltages. A T-type H-bridge circuit is adopted to implement the proposed balancing technique. The gate pulses to generate the five-level output are obtained by employing sine-triangle comparison technique. Finally, the simulation results are presented to cope up with the proposed balancing scheme.

Keywords— T-type converter, voltage balancing, pulse width modulation

1. Introduction

Multilevel converters are attracting more attention in high-voltage and high-power electronic applications, since an improved high output voltage can be obtained with a respective harmonic content reduction [1]-[5]. A lot of multilevel topologies have been proposed in the past thirty years. The most common topologies are the diode-clamped, capacitor-clamped and cascaded types. In order to operate the switches in the above-mentioned topologies, switching schemes such as pulse width modulation (PWM), space vector pulse width modulation (SVPWM), selective harmonic elimination pulse width modulation (SHEPWM), nearest level modulation (NLM) and so on are effective solutions [6], [7]. To satisfy specific application requirements or to improve the operating performance, modifications and combinations of common topologies have been suggested. One of them is a T-type converter [8]-[12]. It is known that the T-type converter is more efficient than other multilevel converter topologies up to the medium switching frequency range.

The proposed method offers high degree of flexibility to operate in any range of modulation index (m_a). The benefits of a reduced number of switching devices, a reduced number of dc power supplies enables the T-type converter to suit for various industry applications. This script is detailed as follows: IInd Section explores the operation of the proposed inverter, and its operating modes, in Section III, the modulation scheme is presented, in IVth Section, the DC-link voltage balance problem is addressed. Simulation results are presented in Vth Section, Section VI discusses the conclusion.

2. System Configuration

Fig. 1 shows the proposed single-phase T-type inverter. It consists of four IGBTs (T1-T4) with anti-parallel diodes. The DC-link consists of single DC source parallel to two series-connected dc capacitors. The mid-point terminal of the DC-link is connected to the H-bridge circuit through a branch consisting of four diodes and an IGBT. This mid-

point branch is capable of bi-directional voltage blocking and bi-directional conducting.The dc supply can be obtained either from rectifier circuits, battery banks, or pv arrays.

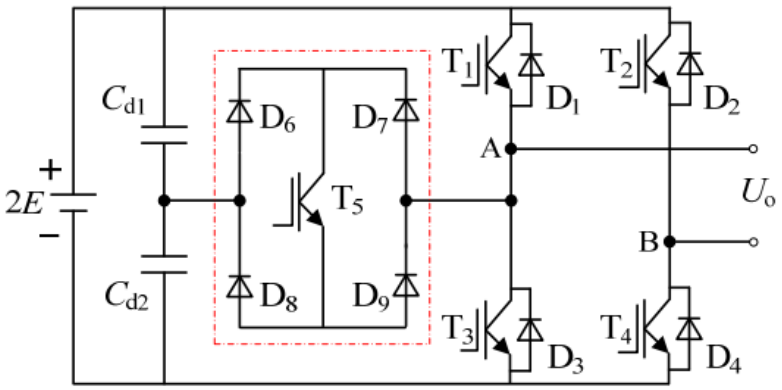


Fig. 1. Circuit diagram of a T-type five-level inverter.

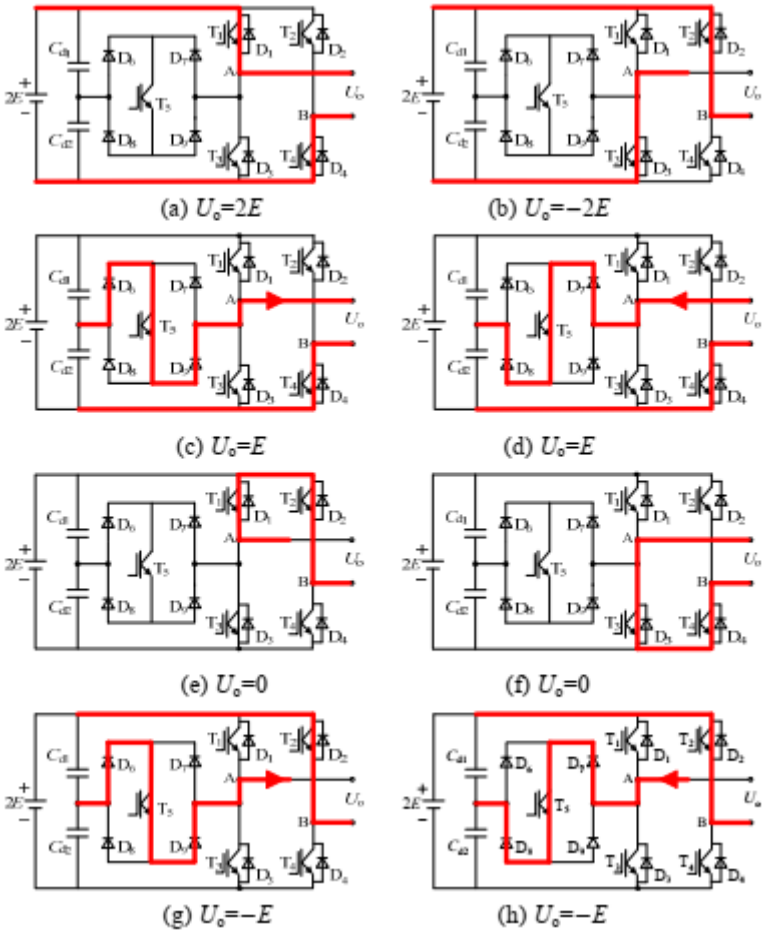


Fig. 2. Operating modes.

Fig. 2(a) gives U_0 = 2E, this switching state is the peak-level operating mode. During this state, the devices T1 and T4 conducts. Fig. 2(b) gives U_0 = -2E, this switching state is the negative peak-level operating mode. During this state, the devices T2 and T3 conducts. Fig. 2(c) and Fig. 2(d) gives U_0 = E for positive and negative directions of load current, respectively. The devices D6, T5, D9, and T4 conducts for I_o positive. The devices D7, T5, D6, and D4 conducts for I_o negative. Fig. 2(e) and Fig. 2(f) gives U_0 = 0, this is also called zero-level operating mode. During this state, the set of devices T1, T2 and T3, T4 are effectively utilized. Fig. 2(g) and Fig. 2(h) gives U_0 = -E for positive and

negative directions of load current, respectively. The conducting devices during this mode are listed in Table 1.

3. Sinusoidal PWM Scheme

Table 1 lists the various switching states of the proposed converter operating in seven-level mode. The digital numbers 1 and 0 is the indication for switch-on and switch-off respectively for the switches shown in Fig. 1. It can be observed that the switches S_1 and S_2 are operating at lower switching frequencies that results in lower switching losses. Fig. 3 shows the modulation method [13-14] to generate the gate pulses to the switches in the proposed converter. A regular sinusoid is cross-compared with six level-shifted triangular waves to produce the seven-level PWM output voltage. The Modulation Index (*M.I.*) that determines the number of output levels is defined as follows:

$$M.I. = \frac{V_{0peak}}{3 \times V_{dc}} \quad (1)$$

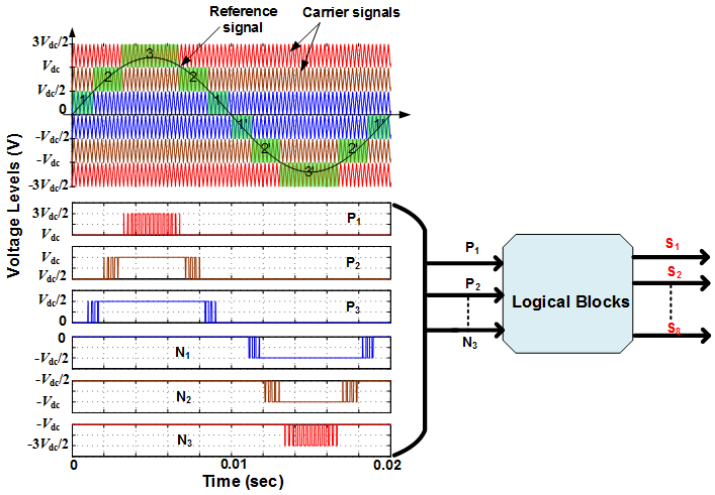


Fig. 3. Sine-triangle comparison PWM scheme.

Table 1. Switching Sequence of the inverter

Output Voltage (U_o)	Conducting devices	
	$I_o > 0$	$I_o < 0$
2E	T1, T4	D1, D4
E	D6, T5, D9, and T4	D7, T5, D6, and D4
0	T1, T2	T3, T4
-E	D2, D6, T5, D9	D7, T5, D8, T2
2E	T2, T3	D2, D3

Table 2. Configuration Parameters

Parameters	Values
V_{dc}	240 V
P_{output}	730 W, 335 W
V_0	230 V
I_0	3.5 A
Switching frequency (f_{sw})	4 kHz
Fundamental frequency (f_{sw})	50 Hz

4. DC-link Balancing Scheme

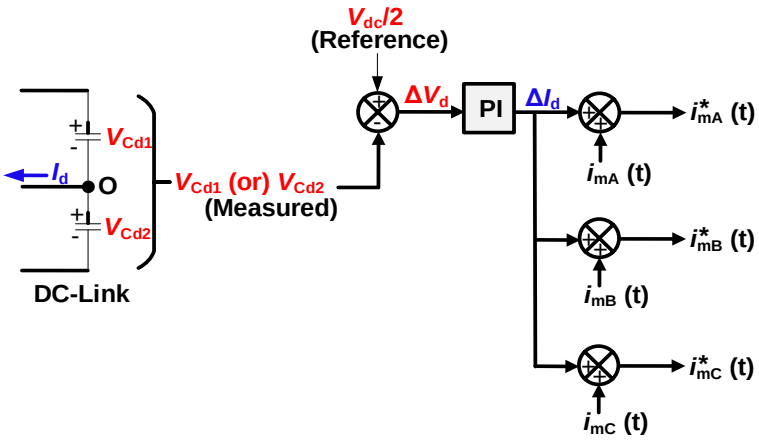
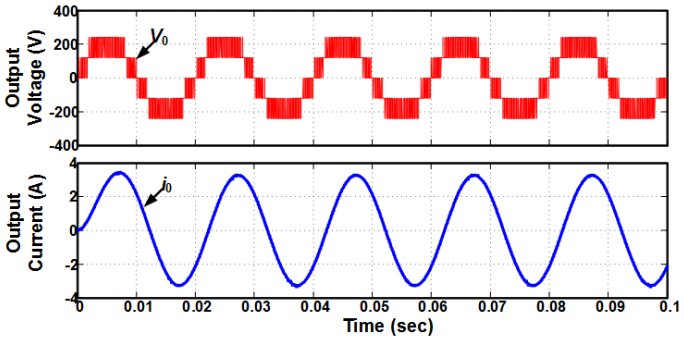


Fig. 4. Block-diagram of the DC-link Capacitor Voltage Control.

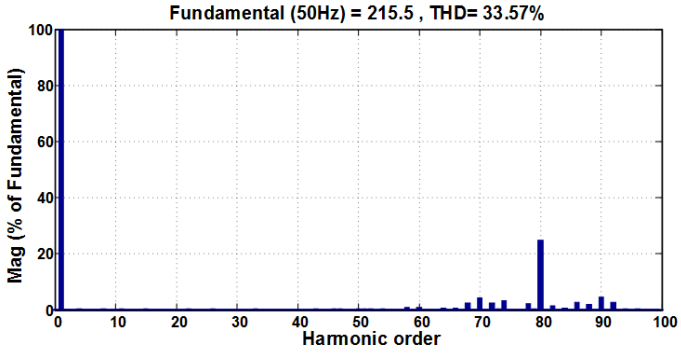
The balancing of the DC-link capacitor voltages is essential to improve the quality of the output. The given single DC supply (V_{dc}) is split into two voltages ($V_{dc}/2$ and $V_{dc}/2$) across the DC-link capacitors (C_{d1} and C_{d2}). In order to balance the DC-link capacitor voltages (V_{Cd1} and V_{Cd2}), a simple controller is developed and its offset error is added with the reference fundamental signals. Fig. 3.7 depicts the developed control strategy to balance the DC-link capacitor voltages. It can be noted that this controller can be implemented with the measurement of the voltage across one of the DC-link capacitors in order to maintain the desired voltage magnitude of $V_{dc}/2$.

5. Simulation Results

The simulation parameters are considered to produce a single-phase output voltage of 230 V and 50 Hz. The other values of the parameters considered for simulation work are listed in Table 2. Fig. 5(a) shows the inverter output results for an M.I. of 0.9. The inverter is producing a 5-level output at M.I. = 0.9. Figs. 5(b) and 5(c) illustrate the harmonic analysis of the inverter output voltage and current respectively. It can be observed that when the inverter is operating at M.I. = 0.9, the magnitude of the peak value of the fundamental component of the output voltage is 215 V and the %Total Harmonic Distortion (%THD) is 33.5. Fig. 6(d) illustrates the DC-link capacitor voltages of the T-type converter using proposed balancing technique. It can be observed that, when the controller is off, the capacitor voltages are distorted and when the controller comes into action, the capacitor voltages are equal an balanced. This shows the abiliy of the controller shown in Fig. 4 in balancing the DC-link capacitor voltages.



(a)



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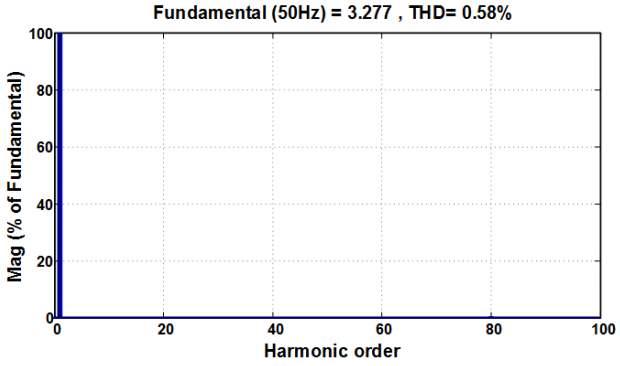
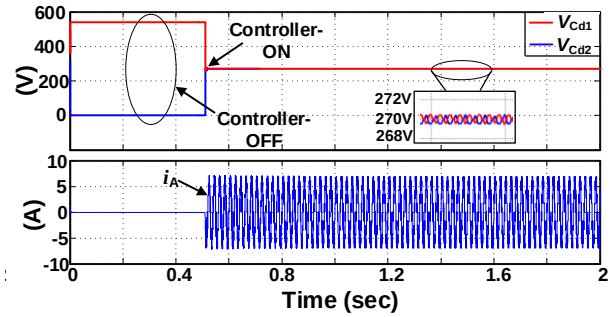


(c)



(d)

Fig. 5. Simulation outcomes at *M.I. = 0.9*: (a) System voltage and current waveforms at the output, (b) FFT analysis of V_0, (c) FFT analysis of I_0, and (d) DC-link capacitor voltage using the proposed balancing technique.

6. Conclusion

This paper proposes a balancing method to control the dc-link capacitor voltages of a T-type converter. The proposed method uses reduced number of auxiliary components to produce equal capacitor voltages. The proposed method is effective in balancing the capacitor voltages at any value of modulation index. The operating modes of the converter, PWM technique, and the complete balancing technique is presented in detail. The effectives of the topology and the balancing method are shown using MATLAB/SIMULINK environment.

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