A Seven-Level Quasi Z-source Inverter

[1]Sk. Nazeer, [2]M. Sneha, [3]B. Surendra, [4]K. Ravi Kumar Reddy, [5]T. Abhilash, [6]A.Yadagiri

[1,2,3,4]Department of Electrical and Electronics Engineering
Aditya Engineering College, Surampalem, Andhra Pradesh
[5]Accendere Knowledge Management Services,
[6]Department of Electrical and Electronics Engineering, MLR Institute of Technology, Hyderabad

Email:
[1]sknazeer082@gmail.com,[2]snehamadireddy1999@gmail.com,[3]bodapatisurendra05@gmail.com, [4]ravikumarreddy.eee@gmail.com
[5]abhilash.tripuathi@accendere.co.in, [6]yadagiri259@gmail.com

Abstract— A seven-level inverter with quasi Z-source boost converters is proposed in this paper. The proposed topology employs a packed U-cell asymmetrical type multilevel inverter along withfront end quasi Z-source networks. The quasi networks provides high gain compared to a conventional boost converter. This topology is most suitable photovoltaic multi-string applications. The proposed topology has the potential to supply both the DC and AC type loads. The inverter structure has lower number of active switches which helps in reduction of losses and improvement in efficiency. In this paper, theoperation principle of quasi network and inverter circuit are explained in detail. In addition,the simulation results for various modulation indices are presented.The proposed topology is gated using sinusoidal Pulse Width Modulation in MATLAB/Simulink environment.

Keywords— quasi network, multilevel inverter, seven-level

1. Introduction

The evolution of Z-source inverters(ZSIs) [1] in the area of power electronics has seen a significant rise in the lastdecade due to its wide range of applications in major areas like uninterruptible power supply (UPS), facts, hybrid electrical vehicles [2],and distributed generation (DG). The limitations of voltage source inverters (VSIs) and current sourceinverters (CSIs) are addressed through flexible control of output voltage by allowing overlap of switches for a part ofswitching cycle, which eliminates the need of dead band between the switches, thus reducing the waveform distortionand enhancing reliability. In addition, it provides single-stage power conversion with buck-boost capability, thusimproving the efficiency of the system compared with two-stage conversion due to reduced component count.A comprehensive survey on differentZ-source topologies and their advancements is reported in [3].

In contemporary, multilevel inverter (MLI) is becoming popular for low-voltage and low-power applications. It offerssignificant advantages of lower device ratings, low dv/dt, low total harmonic distortion (THD), and reduced filter size.Some well-known and popular topologies are neutral-point-clamped MLIs (NPC MLIs), flying capacitor MLIs (FCMLIs), and cascaded H-bridge MLIs (CHB MLIs). Among these, CHB is most preferred due to its modularity feature [4].Moreover, several topologies are developed in recent years in terms of reduced component count, capacitor voltagebalancing, control complexity, and the number of direct current (dc) sources. However, the switch count remains amajor constraint in developing new topologies. Despite the various advantages, the output gain of MLI is buck innature, which is a limitation. This necessitates a suitable power conditioner to be upgraded with MLI in order toimprove input voltage regulation as well as output voltage gain. Therefore, MLI is upgraded with impedance source network with features of improved output voltage gain, enhanced reliability, enhanced input voltage regulation, and quality output waveforms for the increase in levels.

The proposed converter offers the benefits of higher voltage gain and seven-level AC output with a reduced number of switching devices, a reduced number of dc power supplies, and lower off-state voltage stress across the switching devices. This script is detailed as follows: IInd Section explores the operation of the proposed inverter, and its operating modes, in Section III, the

modulation scheme with improved spectral performance is shown, in IVth Section, the simulation results at different values of modulation indices are discussed and Vth Section, discusses the conclusion.

2. System Configuration

Fig. 1 shows the proposed single-phase seven-level quasi z-source based MLI using packed u-cell structure. The z-source network is formed by the elements called inductors, diodes capacitors and an active switch. The inverter circuit consists of 6 active switching devices with bi-directional conducting capability. The dc supplies can be obtained either from rectifier circuits, battery banks, or pv arrays.

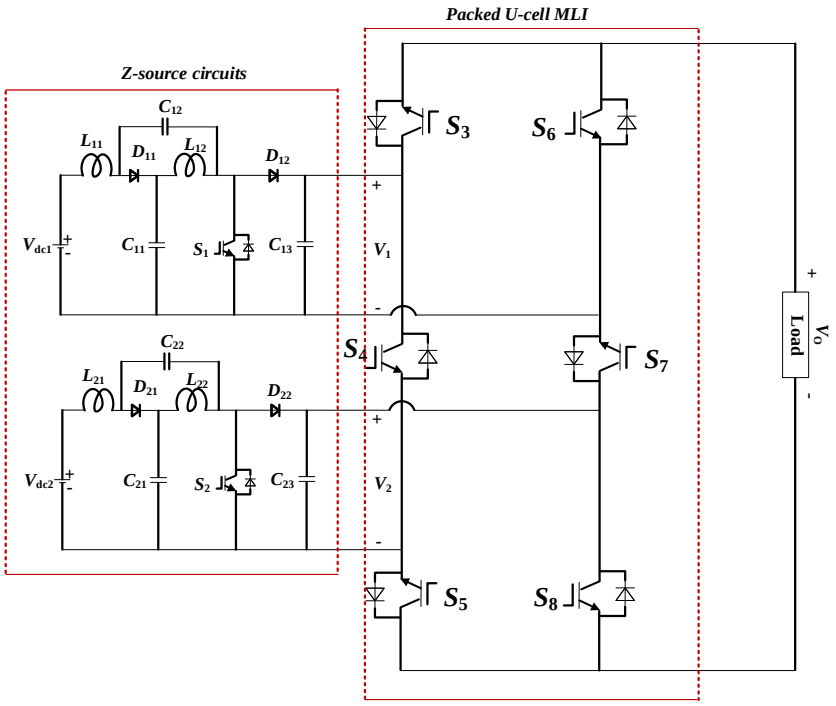
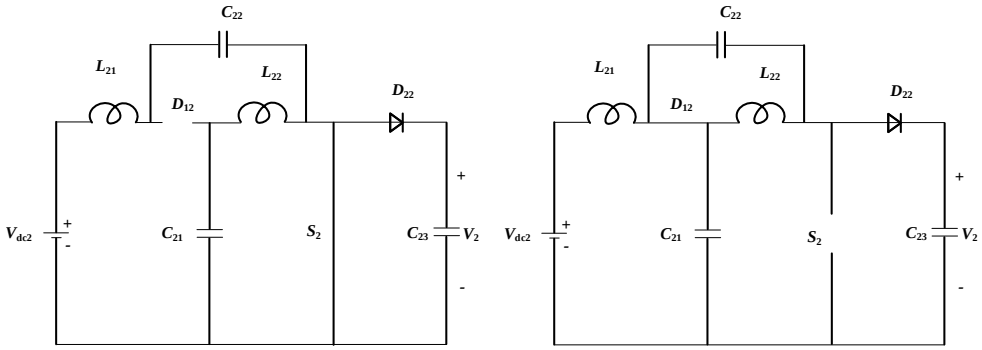
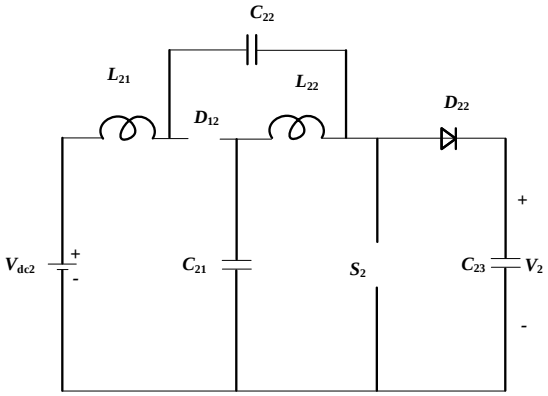


Fig. 1. Circuit diagram of the proposed configuration.



(a) (b)



(c)

Fig. 2. Operating states of Z-source network: (a) shoot through state,(b) active state,(c) discontinuous state.

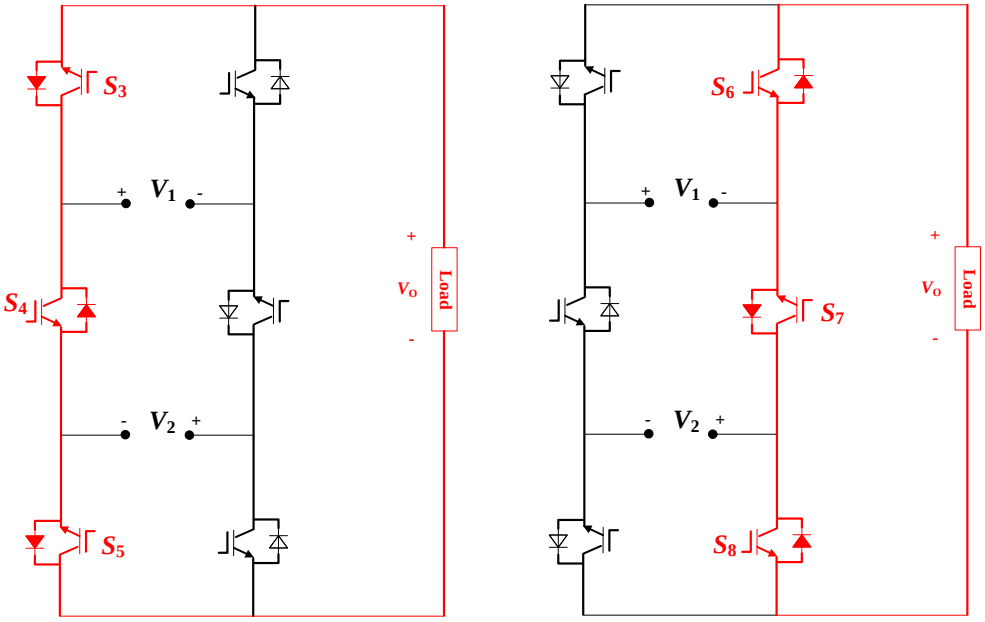
The quasi Z-source network during shoot through and active states are shown in Figs. 2 (a) and (b) respectively. During shoot through state, switch (S1) is turned-on. This creates two shoot through current paths for the DC source (Vdc2). The first path is through Vdc2-L21-C22-S2 and the second path is through Vdc2-L21-C22-D22-C23. Hence, the total dc source current is the sum of the currents in the first and second paths. The total time interval per cycle (T) is divided into two parts. Active-state time (T_A) and shoot-through state time (T_S).

$$T = T_A + T_S \tag{1}$$

The quasi Z-source networks operate in such a way that they produce the output dc voltages V1 = Vdc and V2 = 2Vdc.

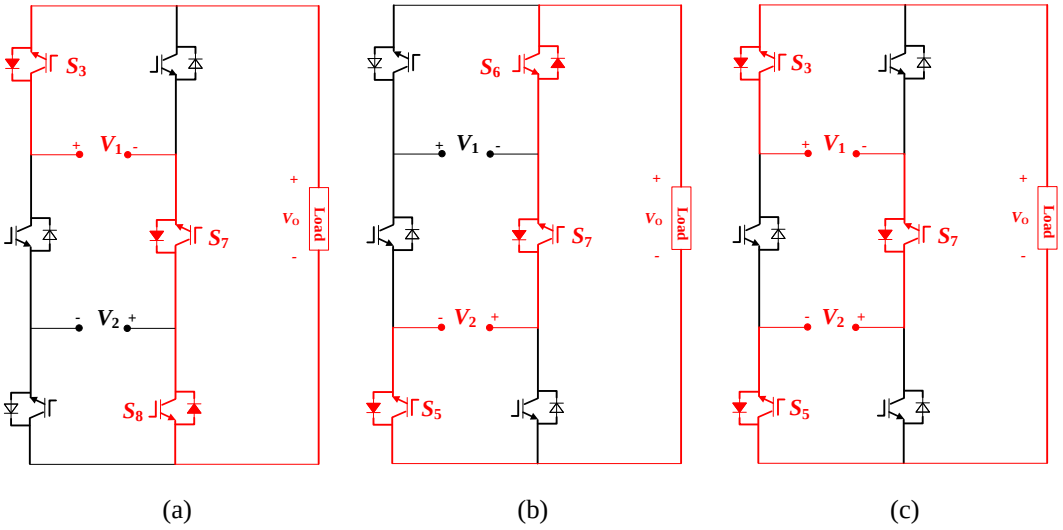
Figs. 3(a) and (b) gives the operating modes of the inverter circuit during V_0 = 0- and V_0 = 0+, respectively.These switching state gives the zero output voltage level across the R-L load. Fig. 4 (a) shows the operating state that produces V0 = V1 = Vdc. Fig. 4 (b) shows the operating state that produces V0 = V2 = 2Vdc. Similarly, Fig. 4 (c) shows the operating state that produces V0 = V1+V2 = 3Vdc. This completes the operating states of zero and positive output voltage levels.

Fig. 5(a) shows the operating state that produces V0 = -V1 = -Vdc. Fig. 4 (b) shows the operating state that produces V0 = -V2 = -2Vdc. Similarly, Fig. 4 (c) shows the operating state that produces V0 = -(V1+V2) = -3Vdc. This completes the operating states of negative output voltage levels.



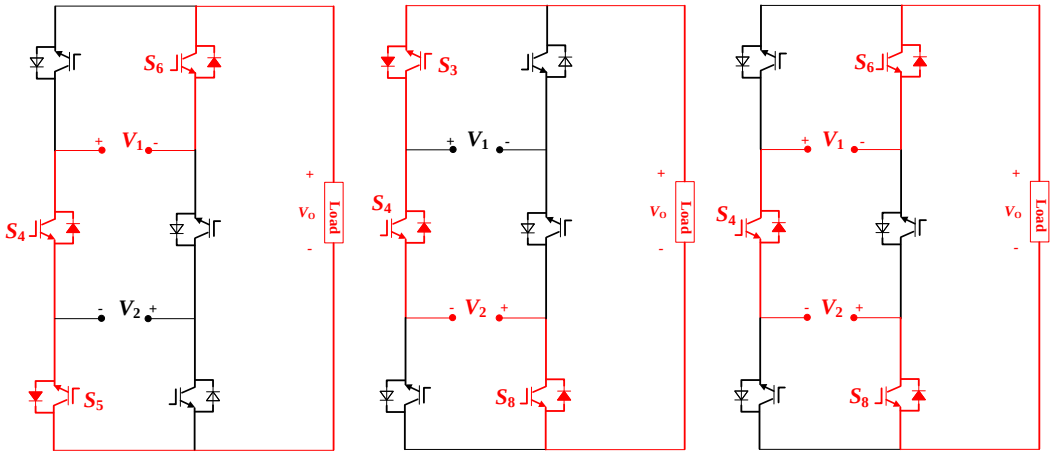
(a) (b)

Fig. 3. Operating states of PUC MLI: (a) V0 = 0-(b) V0 = 0+.



(a) (b) (c)

Fig. 4. Positive operating states of PUC MLI: (a) V0 = V1,(b) V0 = V2, (c) V0 = V1+V2.



(a) (b) (c)

Fig. 5. Negative operating states of PUC MLI: (a) V0 = -V1,(b) V0 = -V2, (c) V0 = -(V1+V2).

3. Sinusoidal PWM Scheme

Table 1 lists the various switching states of the proposed converter operating to produce seven-level output. The digital numbers 1 and 0 is the indication for switch-on and switch-off respectively for the switches shown in Fig. 1. It can be observed that the switches S_4 and S_7 are operating at lower switching frequencies that results in lower switching losses. Fig. 3 shows the modulation method [13-14] to generate the gate pulses to the switches in the proposed converter. A regularsinusoid is cross-compared with six level-shifted triangular waves to produce the seven-level PWM output voltage. The Modulation Index (*M.I.*) that determines the number of output levels is defined as follows:

$$M.I. = \frac{V_{0peak}}{3 \times V_{dc}} \quad (1)$$

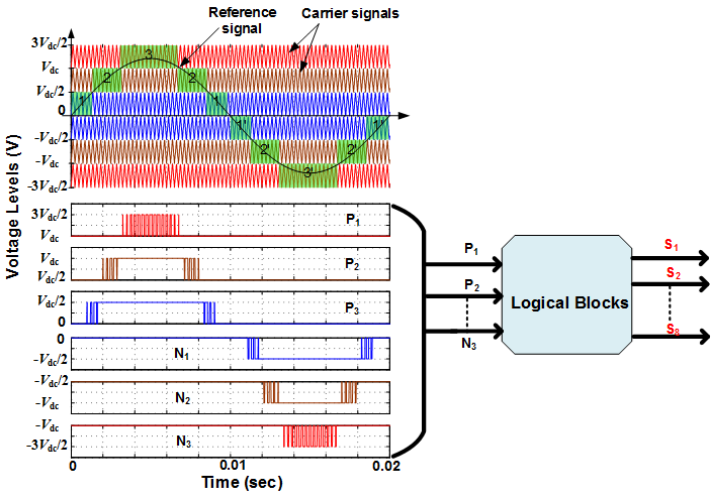


Fig. 3. Sine-triangle comparison PWM scheme.

Table 1. Switching Sequence of the Inverter

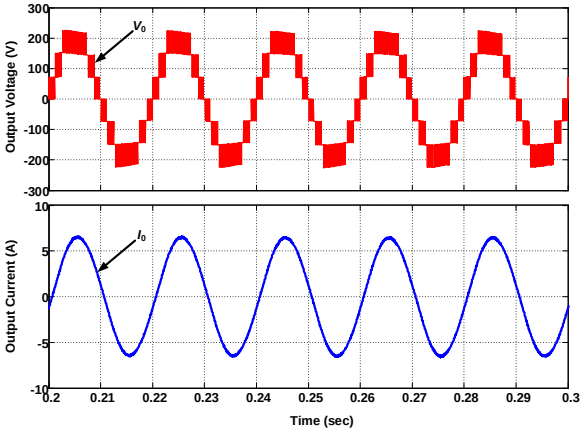
Output Voltage (V_0)	**Conducting Devices**
3Vdc	S3, S7 and S5
2Vdc	S6, S7 and S5
Vdc	S3, S7 and S8
0+	S6, S7 and S8
0-	S3, S4 and S5
-Vdc	S6, S4 and S5
-2Vdc	S3, S4 and S8
-3Vdc	S6, S4 and S8

Table 2. Configuration Parameters

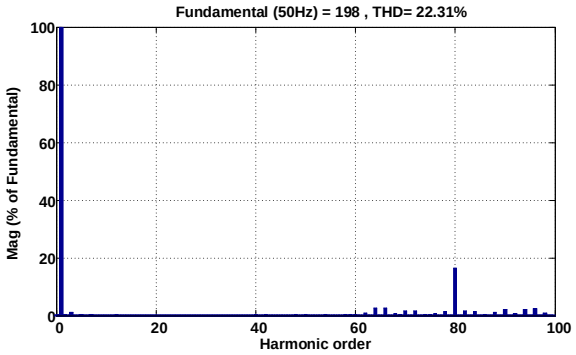
DC Voltages (Vdc1, Vdc2)	30 V, 60 V
Inductors	0.5 mH
Capacitors (C11, C12, C21 and C22)	500 µF
Filter Capacitors (C13 and C23)	2000 µF
Switching frequency of qZs-network	10 kHz
Carrier wave frequency of MLI	4 kHz
Fundamental output frequency	50 Hz
Rated output Power	500 W

4. Simulation Results

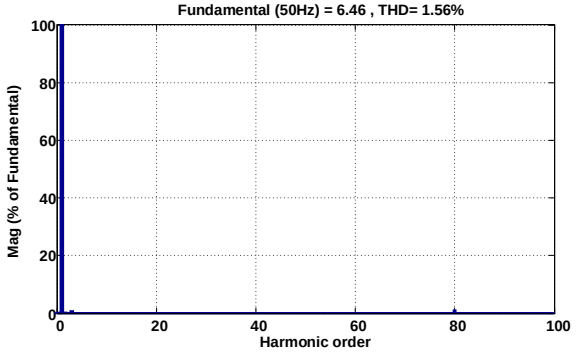
The simulation parameters are considered to produce a single-phase output voltage of 230V and 50 Hz. The other values of the parameters considered for simulation work are listed in Table 2. Figs. 4(a) and 5(a) show the inverter output results for an M.I. of 0.9 and 0.6 respectively. The inverter is producing 7-level output at M.I. = 0.9 and five-level output at M.I. = 0.6. Due to the reduction in the value of M.I., the peak value of the output also decreases. Figs. 4(b) and 5(b) illustrate the harmonic analysis of the inverter output voltage. It can be observed that when the inverter is operating at M.I. = 0.9, the magnitude of the peak value of the fundamental component of the output voltage is 323 V and the %Total Harmonic Distortion (%THD) is 22.4. It is also to be noted that the decrease in the value of M.I. increases %THD. Figs. 4(c) and 5(c) illustrate the harmonic analysis of the inverter output current. It can be observed that when the inverter is operating at M.I. = 0.9, the magnitude of the peak value of the fundamental component of the output current is 4.9A and the %THD is 0.38. Due to the reduction in the value of M.I. the peak value of the fundamental component of the output current is reduced to 3.2 A and the %THD is slightly increased to 0.58.



(a)

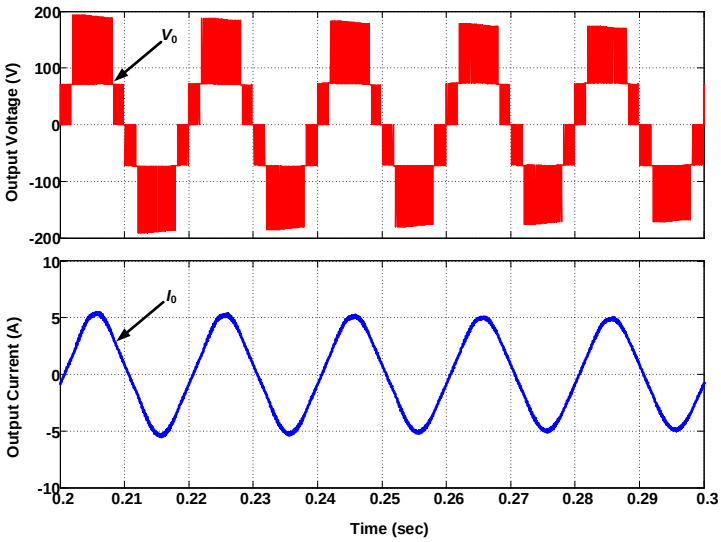


(b)

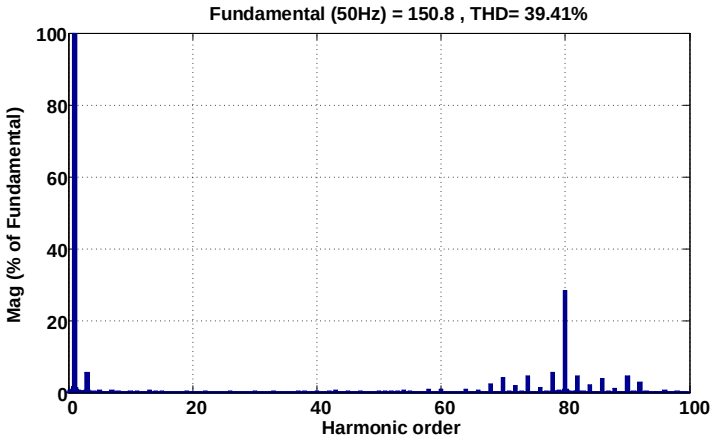


(c)

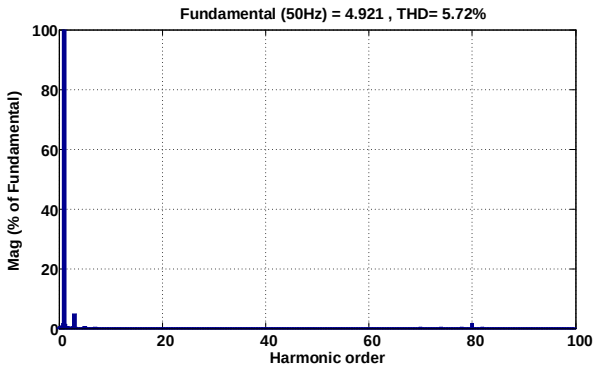
Fig. 4. Simulation results at *M.I. = 0.9*: (a) Output voltage and current waveforms, (b) FFT analysis of V_0, and (c) FFT analysis of I_0.



(a)



(b)



(c)

Fig. 5. Simulation results at *M.I. = 0.6*: (a) Output voltage and current waveforms, (b) FFT analysis of V_0, and (c) FFT analysis of I_0.

5. Conclusion

This paper provides a detailed analysis of the seven-level operating modes of the proposedquasi Z-source based MLi withreduced component. The proposed topology is a two-stage circuit that provides independent control of the output variables.The modulation technique to generate the firing pulses to the inverter switches has been elaborated. The simulation results at different values of M.I. and at different power ratings are presented. FFT analysis of the output

parameters has been carried out and it is noted that the %THD of the current waveforms are within the limits of the IEEE 1547 grid standard.

REFERENCES

[1] F. Z. Peng, "Z-source inverters," In: Wiley Encyclopedia of Electrical and Electronics Engineering. pp. 1-11, 1999.

[2] C. M. Lai, Y. H. Cheng, M. H. Hsieh, Y. C. Lin, "Development of a bidirectional DC/DC converter with dual-battery energy storage for hybrid electric vehicle system," *IEEE Trans Vehicular Technology*, vol. 67, no. 2, pp. 1036-1052, 2018.

[3] Y. P. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, G. E. Town,"Impedance source network for electric power conversion—part I: a topologicalreview,"*IEEE Trans Power Electron*,vol. 30, no. 2, pp. 699-716, 2015.

[4] S. K. Maddugari, V. B. Borghate, S. Sabyasachi,"A reliable and efficient single-phase modular multilevel inverter topology,"Int J Circ TheorAppl. vol. 47, no. 5, pp. 718-737, 2019.

[5] T. A. Meynard, and H. Foch, "Multi-level choppers for high voltage applications," *European Power Electronics and Drives Journal*, vol. 2, no. 1, pp. 45-50, 1992.

[6] T. Abhilash, A. Kirubakaran, and V. T. Somasekhar, "A Seven-Level VSI with a Front-end Cascaded Three-Level Inverter and Flying Capacitor fed H-Bridge", *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 6073-6088, 2019.

[7] Y. Ounejjar, K. Al-Haddad, and L. A. Dessaint, "A novel six-band hysteresis control for the packed U cells seven-level converter: Experimental validation," *IEEE Trans. Ind. Electron.*, vol. 59, no. 10, pp. 3808–3816, Oct. 2012.

[8] M. Saeedifard, P. M. Barbosa, and P. K. Steimer, "Operation and control of a hybrid seven-level converter," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 652–660, Feb. 2012.

[9] H. Vahedi and K. Al-Haddad, "Real-time implementation of a sevenlevel packed U-cell inverter with a low-switching-frequency voltage regulator," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5967–5973, Aug. 2016.

[10] W. Sheng and Q. Ge, "A novel seven-level ANPC converter topology and its commutating strategies," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7496–7509, Sep. 2018.

[11] A. Tsunoda, Y. Hinago, and H. Koizumi, "Level and phase shifted PWM for 7-level switched-capacitor inverter using series/parallel conversion," *IEEE Trans. Ind. Electron.*, vol. 61, no. 8, pp. 4011–4021, Aug. 2014.

[12] J.-C. Wu and C.-W. Chou, "A solar power generation system with a sevenlevel inverter," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3454–3462, Jul. 2014.

[13] T. Abhilash, A. Kirubakaran, and V. T. Somasekhar, "A New Structure of Three-Phase Five-Level Inverter With Nested Two-Level Cells," *Int. J. of Circuit Theory and Appl., Wiley*, vol. 47, no. 9, pp. 1435-1445, 2019.

[14] T. Abhilash, A. Kirubakaran, and V. T. Somasekhar "A new hybrid flying capacitor based single phase nine-level inverter", *Int.Trans. Electrical Energy Systems, Wiley*, vol. 29, no. 12, pp. 1-15, 2019.