Analysis and Simulation of a Novel H-Bridge based Multi-Level Inverter with reduced DC sources

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Abstract— In this manuscript, a seven-level inverter topology using novel bridge structure with the minimum component count is presented. This configuration is gifted to enhance the number of output voltage levels by using a fewer number of power electronic evices such as switches, power diodes, driver circuits, and dc voltage sources that lead to saving of installation space and cost of the topology. In addition, in the proposed cascaded multilevel inverter, not only the number of required power electronic devices is reduced, but also the amount of the blocked voltage by switches, and the number of different voltage amplitudes of the used sources is decreased. The operating modes of the proposed inverter are analyzed in detail during zero, positive, and negative levels. The proposed topology is gated using sinusoidal Pulse Width Modulation in MATLAB/Simulink environment.

Keywords— multilevel inverter, seven-level, pulse width modulation

1. Introduction

Conventional multilevel topologies, such as the neutral point clamped converter (NPCC), flying capacitor converter (FCC), cascaded H-bridge converter (CHBC), as well as the modular multilevel converter (MMC), have been well studied and commercialized in the past decades [1-3]. However, when the voltage levels increase, the number of clamping diodes in the NPCC and flying capacitors (FCs) in the FCC rises tremendously [4,5]. Furthermore, the NPCC suffers from indirect clamping of the inner devices when the voltage level is higher than three [4]. The CHBC and MMC are easier to expand the voltage levels due to their modular design [5]. But the CHBC needs a phase-shifting transformer to provide isolated DC sources, which results in substantial investment and volume [6-9]. The MMC shows good prospects for HVDC transmission. But the complex controls (e.g., capacitor voltage balancing control and circulating current suppression control) and relative high primary investment make the MMC less attractive in medium-voltage applications [10-12].The proposed converter offers the benefits of a reduced number of switching devices, a reduced number of dc power supplies, and lower off-state voltage stress across the switching devices. This script is detailed as follows: IInd Section explores the operation of the proposed inverter, and its operating modes, in Section III, the modulation scheme with improved spectral performance is shown, in IVth Section, the simulation results at different values of modulation indices are discussed and Vth Section, discusses the conclusion.

2. System Configuration

Fig. 1 shows the proposed single-phase seven-level inverter using switching devices, and dc-sources. All the switching devices used in the proposed configuration are of bi-directional conducting devices with uni-directional voltage sustaining ability. The dc supplies can be obtained either from rectifier circuits, battery banks, or pv arrays. The proposed topology consists of two dc sources V_{dc1} and V_{dc2}.In order to produce the seven-level output, the dc source magnitudes are to be chosen as $V_{dc1} = V_{dc}$ and $V_{dc2} = 2\ V_{dc}$. It should be noted that the dc sources are aligned in opposite direction w.r.t each other.

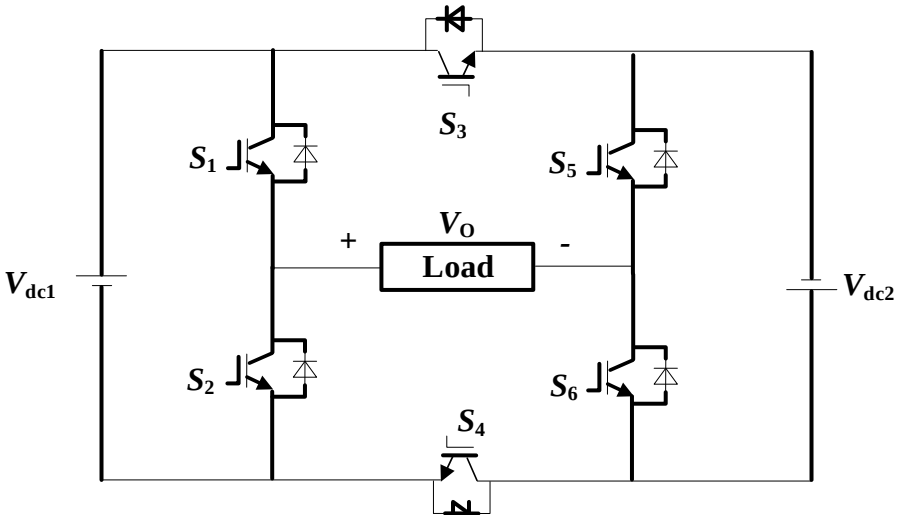
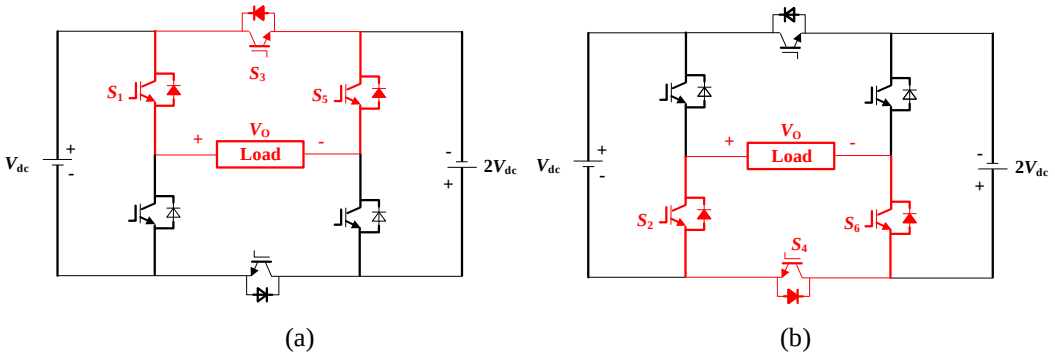
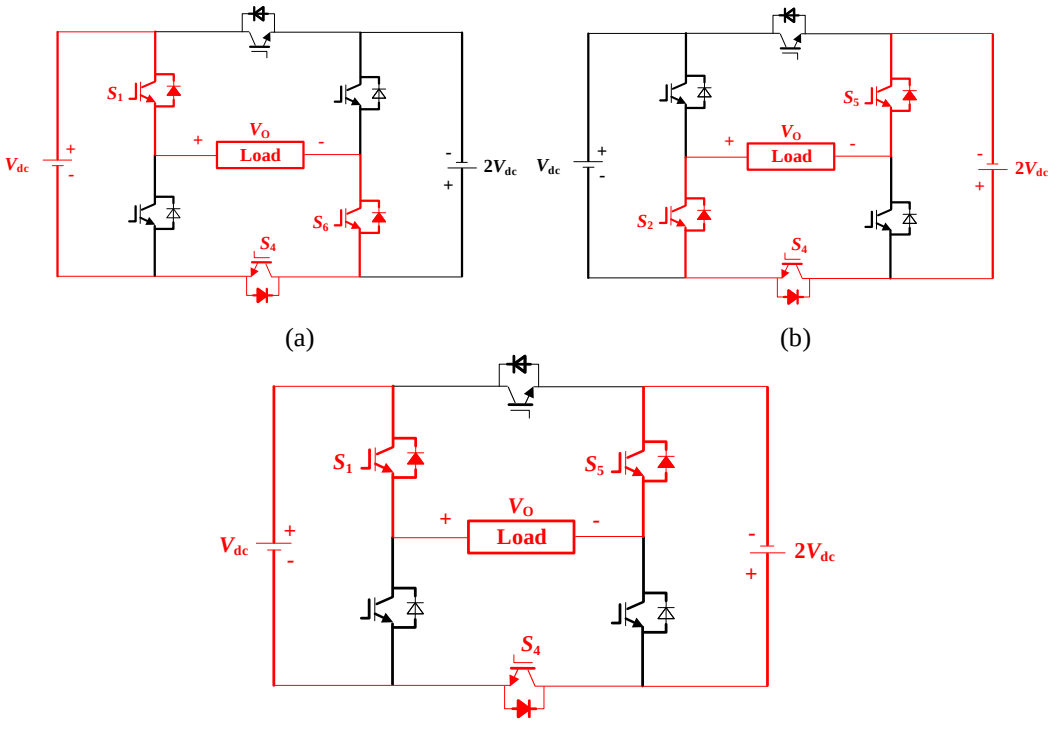


Fig. 1. Circuit diagram of the proposed configuration.



(a) (b)

Fig. 2. Operating states: (a) Positive Zero-crossing(b) Negative Zero-crossing.



(a) (b)

(c)

Fig. 3. Positive-level operating states: (a) $V_O = V_{dc}$,(b) $V_O = 2V_{dc}$ and (c) $V_O = 3V_{dc}$.

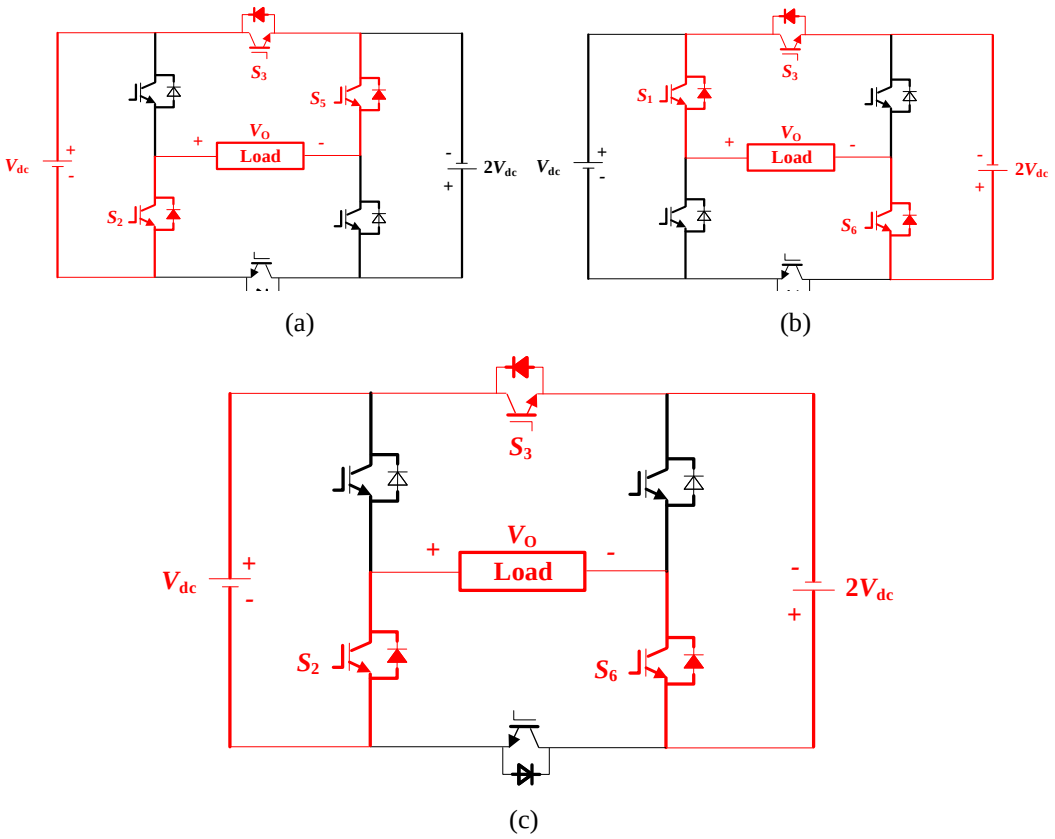


Fig. 4. Negative-level operating states: (a) V_O = -V_{dc},(b) V_O = -2V_{dc} and (c) V_O = -3V_{dc}.

Fig. 2(a) gives $V_0 = 0^+$. During this state, the devices S1, S3, and S5are turned-on. Fig. 2(b) gives $V_0 = 0^-$. During this state, the devices S2, S4, and S6are turned-on. The conduction of either the switch or its anti-parallel diode, depends on the direction of the load current.

Fig. 3(a) gives $V_0 = V_{dc}$. During this state, the devices S1, S4 and S6 conducts. Fig. 3(b) gives $V_0 = 2V_{dc}$, during this state, the devices S2, S4 and S5 conducts. Fig. 3(c) gives $V_0 = 3V_{dc}$, during this state, the devices S1, S4 and S5 conducts.

Fig. 4(a) gives $V_0 = -V_{dc}$. During this state, the devices S2, S3 and S5 conducts. Fig. 3(b) gives $V_0 = -2V_{dc}$, during this state, the devices S1, S3 and S6 conducts. Fig. 3(c) gives $V_0 = -3V_{dc}$, during this state, the devices S2, S3 and S6 conducts.

3. Sinusoidal PWM Scheme

Table 1 lists the various switching states of the proposed converter operating in seven-level mode. The digital numbers 1 and 0 is the indication for switch-on and switch-off respectively for the switches shown in Fig. 1. It can be observed that the switches S_3 and S_4 are operating at lower switching frequencies that results in lower switching losses. Fig. 5 shows the modulation method [13-14] to generate the gate pulses to the switches in the proposed converter. A regular sinusoid is cross-compared with six level-shifted triangular waves to produce the seven-level PWM output voltage. The Modulation Index (*M.I.*) that determines the number of output levels is defined as follows:

$$M.I. = \frac{V_{0peak}}{3 \times V_{dc}} \quad (1)$$

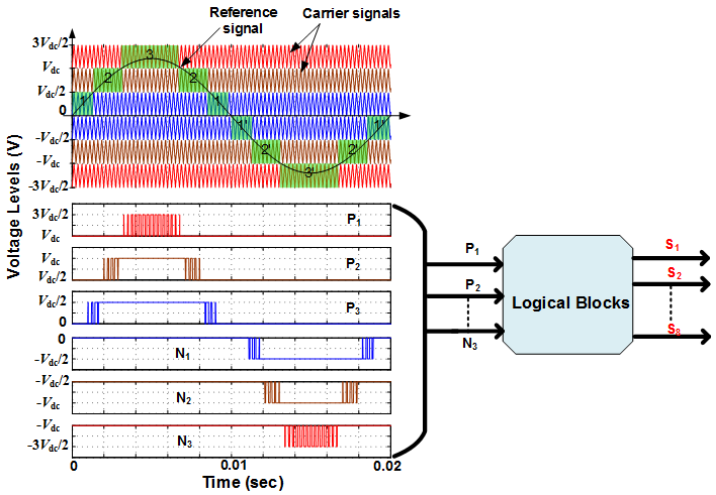


Fig. 5. Sine-triangle comparison PWM scheme.

Table 1. Switching Sequence of the Inverter

Output Voltage (V_0)	**Conducting Devices**
$3V_{dc}$	S1, S4 and S5
$2V_{dc}$	S2, S4 and S5
V_{dc}	S1, S4 and S6
0^+	S1, S3 and S5
0^-	S2, S4 and S6
$-V_{dc}$	S2, S3 and S5
$-2V_{dc}$	S1, S3 and S6
$-3V_{dc}$	S2, S3 and S6

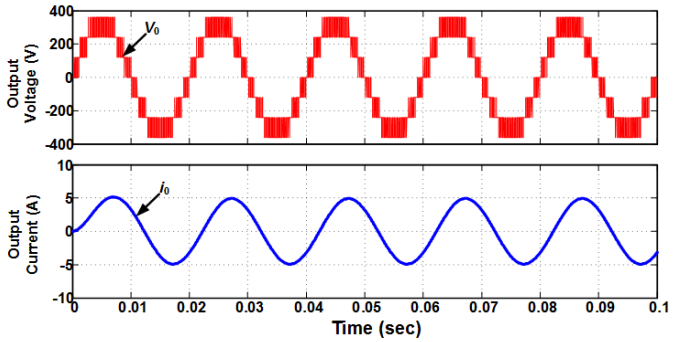
Table 2. Configuration Parameters

Parameters	**Values**
V_{dc}	240 V
P_{output}	730 W, 335 W
V_0	230 V
I_0	3.5 A
Switching frequency (f_{sw})	4 kHz
Fundamental frequency (f_{sw})	50 Hz

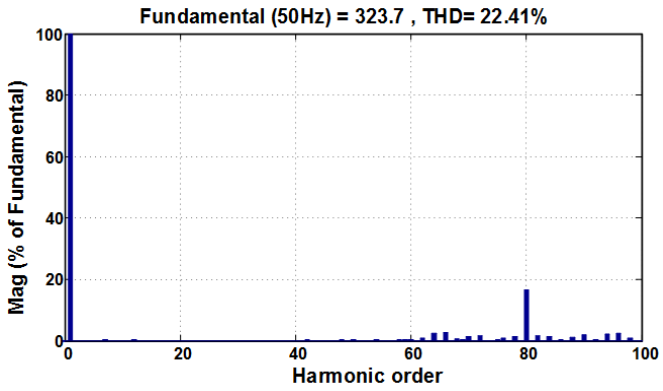
4. Simulation Results

The simulation parameters are considered to produce a single-phase seven-level output voltage of 230 V and 50 Hz. The other values of the parameters considered for simulation work are listed in Table 2. Figs. 6(a) and 7(a) show the inverter output results for an M.I. of 0.9 and 0.6 respectively. The inverter is producing 7-level output at M.I. = 0.9 and five-level output at M.I. = 0.6. Due to the reduction in the value of M.I., the peak value of the output also decreases. Figs. 6(b) and 7(b) illustrate the harmonic analysis of the inverter output voltage. It can be observed that when the inverter is operating at M.I. = 0.9, the magnitude of the peak value of the fundamental

component of the output voltage is 323 V and the %Total Harmonic Distortion (%THD) is 22.4. It is also to be noted that the decrease in the value of M.I. increases the %THD. Figs. 6(c) and 7(c) illustrate the harmonic analysis of the inverter output current. It can be observed that when the inverter is operating at M.I. = 0.9, the magnitude of the peak value of the fundamental component of the output current is 4.9 A and the %THD is 0.38. Due to the reduction in the value of M.I. the peak value of the fundamental component of the output current is reduced to 3.2 A and the %THD is slightly increased to 0.58.



(a)



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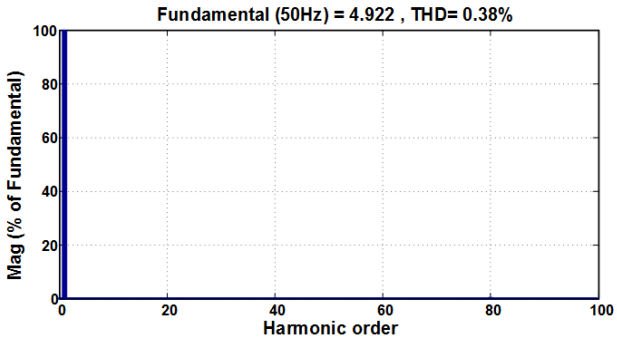
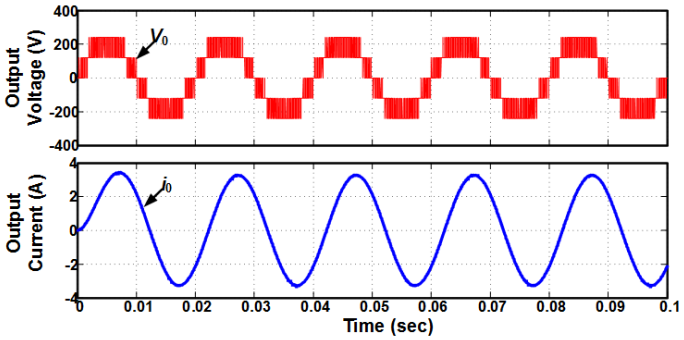
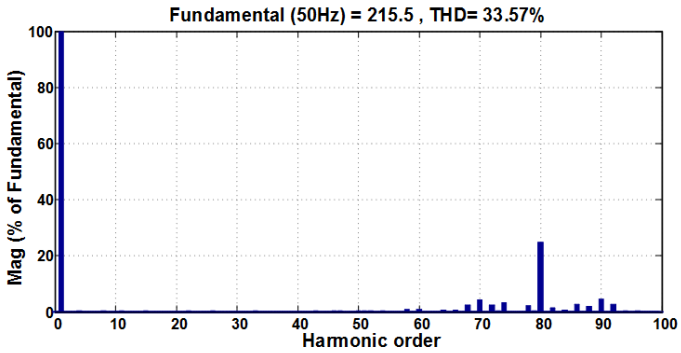


(c)

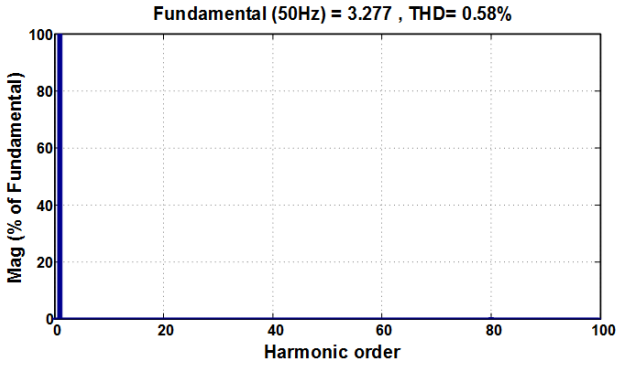
Fig. 4. Simulation outcomes at *M.I. = 0.9*: (a) System voltage and current waveforms at the output, (b) FFT analysis of V_0, and (c) FFT analysis of I_0.



(a)



(b)



(c)

Fig. 5. Simulation outcomes at *M.I. = 0.6*: (a) System voltage and current waveforms at the output, (b) FFT analysis of V_0, and (c) FFT analysis of I_0.

5. Conclusion

This paper provides a detailed analysis of the seven-level operating modes of the proposednovel structure H-bridge based reduced component count MLI. The proposed topology is an improved circuit configuration of H-bridge and T-type MLIs. The modulation technique to generate the firing pulses to the inverter switches has been elaborated. The simulation results at different values of M.I. and at different power ratings are presented. FFT analysis of the output parameters has been carried out and it is noted that the %THD of the current waveforms are within the limits of the IEEE 1547 grid standard.

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